REMARKS

Claims 9, 10, 12, 32-40, 77 and 78 are canceled. The application now contains claims 1-8, 11, 13-31, 41-76 and 79-96. Claims 1-3, 13, 64 and 70-76 are amended. Claims 41-63 and 87-96 are withdrawn from consideration. Applicant reserves the right to pursue the original claims and other claims in this and other applications. A petition for a one-month extension of time is being filed concurrently herewith.

Claims 1, 2 and 70 are rejected under 35 U.S.C. § 102 as being anticipated by Wang. Reconsideration is respectfully requested. Claims 1 and 70, as amended, each recite a "magnetic random access memory device." This is an important aspect of the claimed invention. Wang fails to disclose or suggest the memory device of amended claims 1 and 70. Therefore, the rejection of claims 1 and 70 should be withdrawn. Claim 2 depends from claim 1 and should be allowable along with claim 1 and for other reasons.

Claims 1, 2, 11, 19-22, 64, 65, 70-74 and 76 are rejected under 35 U.S.C. § 103 as being unpatentable over the device shown in Figs. 1 and 2, in view of Wang, further in view of Cassarly, and further in view of Higuchi. Reconsideration is respectfully requested. Claims 1, 64 and 70, as amended, each recite first and second magnetic field shielding materials. According to claim 1, the first material is "in contact with [a] back surface of [a] chip," and the second is "in contact with [a] chip carrier," and a "memory device is located between said first and second . . . materials." Claims 64 and 70 likewise each say that a "memory device is located between . . . first and second layers of magnetic field shielding material."

The prior art references, even when considered in combination, fail to suggest the multiple shielding materials of claims 1, 64 and 70, in the recited locations. None of the references suggest locating a memory device "between" first and second magnetic field shielding materials, as positively recited in the amended claims. Therefore, claims 1, 64 and 70, as amended, should be allowable over the cited prior art. Claims 2-8, 11, 13-31,

64-69, 71-76 and 79-86 depend from claims 1, 64 and 70, respectively, and should be allowable along with the independent claims and for other reasons.

Claim 70 is rejected under 35 U.S.C. § 102 as being anticipated by Tao. Reconsideration is respectfully requested. As noted above, claim 70, as amended, recites a "magnetic random access memory device." Tao fails to disclose or suggest the memory device of amended claim 70. Therefore, the rejection of claim 70 should be withdrawn.

Claim 70 is rejected under 35 U.S.C. § 102 as being anticipated by Maheshwari. Reconsideration is respectfully requested. Maheshwari fails to disclose or suggest the memory device of claim 70. Therefore, the rejection should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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MARK-UP VERSION SHOWING CHANGES MADE

1. (Amended) An integrated circuit structure comprising:

a chip carrier;

at least one integrated circuit chip containing structures which may be affected by external magnetic fields, said integrated circuit chip having a front surface and a back surface, said front surface being supported by [a] said chip carrier, and wherein said structures which may be affected by external magnetic fields include a magnetic random access memory device; [and]

a first magnetic field shielding material in contact with said back surface of said chip; and

a second magnetic field shielding material in contact with said chip carrier, such that said magnetic random access memory device is located between said first and second magnetic field shielding materials.

2. (Amended) The structure of claim 1, wherein said first shielding material is in the form of a first layer of said magnetic field shielding material on said back surface.

3. (Amended) The structure of claim 1, wherein said first shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

13. (Amended) The structure of claim [12] 11, wherein said second magnetic field shielding layer comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

64. (Amended) An integrated circuit structure comprising:

a die carrier;

a die electrically connected to [a] said die carrier, said die being in contact with a first layer of magnetic field shielding material, said die further comprising a magnetic random access memory device; and

a printed circuit board electrically connected to said die carrier, said printed circuit board being in contact with a second layer of magnetic field shielding material, and wherein said magnetic random access memory device is located between said first and second layers of magnetic field shielding material.

70. (Twice Amended) A method of packaging a semiconductor device comprising:

electrically coupling a die carrier to a first surface of a die, said first surface being opposite to a second surface of said die, and wherein said die includes a magnetic random access memory device; [and]

contacting said second surface of said die with a first layer of magnetic field shielding material which shields said die from external magnetic fields, wherein said second surface is a back surface of the die; and

contacting said die carrier with a second layer of magnetic field shielding material which shields said die from external magnetic fields, such that said memory device is located between said first and second layers of magnetic field shielding material.

71. (Amended) The method of claim 70 further comprising the act of electrically coupling said die carrier to a printed circuit board [which has a second layer of magnetic field shielding material].

72. (Amended) The method of claim 71, wherein [said act of contacting said printed circuit board with said second layer of magnetic field shielding material wherein said second] a third layer of magnetic field shielding material is formed on a surface of said printed circuit board.

73. (Amended) The method of claim 72, wherein said [second] third layer of magnetic field shielding material is formed on a top surface of said printed circuit board.

74. (Amended) The method of claim 72, wherein said [second] third layer of magnetic field shielding material is formed on a bottom surface of said printed circuit board.

75. (Amended) The method of claim 72, wherein said [second] third layer of magnetic field shielding material is embedded within said printed circuit board.

76. (Amended) The method of claim 72, wherein said [second] third layer of magnetic field shielding material is formed on both a bottom surface and a top surface of said printed circuit board.